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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/715,264	11/17/2003	Nathan R. Brown	2269-4375.3US (99-1029.03	5086

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EXAMINER	
MACARTHUR, SYLVIA	
ART UNIT	**PAPER NUMBER**
1763	

DATE MAILED: 10/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/715,264	BROWN, NATHAN R.	
	Examiner	Art Unit	
	Sylvia R. MacArthur	1763	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. . The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saka et al (US 6,476,921) in view of Sahota et al (US 5,665,199).

Saka et al teaches a method of polishing a semiconduct using different pressure zones, see abstract and Fig.4.

Re Claims 1, 8, 9: The method of Saka et al teaches selectively applying a plurality of different amounts of pressure to different, selected locations of a backside of the semiconductor device structure and a polishing or planarizing at least one layer of the surface of the semiconductor device structure, see col. 7 lines 1-40.

Re Claims 2, 7, 11, 12: The polishing discussed in Saka et al is CMP according to the title.

Re Claim 6, 13 and 14: The different amounts of pressure are provided by biasing independently movable pressurization structures, see col. 7 lines 1-40 and Fig. 4.

Re Claim 10: The selectively applying a plurality of different amounts of pressure and the polishing or planarizing together effect the formation of a substantially planar surface on the semiconductor device structure, see the abstract.

Re Claims 4,5: At least one raised surface has been located and the adequate pressure applied to planarize see col. 7 lines 1-40.

Re Claim 14: The polishing of Saka et al comprises forming a substantially planar surface on the semiconductor device structure, see abstract.

Saka et al fails to polishing a second semiconductor structure based on the applied pressure of the first.

Sahota et al teaches a methodology of rdeveloping product specific interlayer dielectrid polish processes. Sahota et al illustrates in Fig. 4, the polishing of a first wafer and measuring the topography of that first wafer, then using the first data points to polish a subsequent wafer. Topograsphy (surface profile measurements) is discussed in col. 17 lines 18-26 and col.15 lines 45-67.

The motivation to modify the teachings of Saka et al is to enhance the capabilities of the apparatus from the application of pressure to a specific wafer to wafers in an entire lot or batch. The combined teachings of Saka et al and Sahota et al will increase throughput and the uniformity of polishing with a lot of wafers.

3. Claims 1-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Nagahara et al(US 6,531,397) in view of Sahota et al (US 5,665,199).

Nagahara et al teaches a method of CMP using wafer back pressure differentials, see title.

Re Claims 1, 8, 9: The method of Chen et al teaches selectively applying a plurality of different amounts of pressure to different, selected locations of a backside of the semiconductor device structure and a polishing or planarizing at least one layer of the surface of the semiconductor device structure, see col. 5 and 6

Re Claim 6, 13, and 14: The different amounts of pressure are provided by biasing independently movable pressurization structures see abstract and cols. 5 and 6.

Re Claims 2,7, 11, 12:The polishing discussed in Nagahara et al is CMP according to the title.

Re Claim 10: The selectively applying a plurality of different amounts of pressure and the polishing or planarizing together effect the formation of a substantially planar surface on the semiconductor device structure, see the abstract and cols. 5 and 6.

Re Claims 4, 5: At least one raised surface has been located and the adequate pressure applied to planarize see col. cols. 5 and 6.

Re Claim 14: The polishing of Nagahara et al comprises forming a substantially planar surface on the semiconductor device structure, see abstract.

Nagahara et al fails to polishing a second semiconductor structure based on the applied pressure of the first.

Sahota et al teaches a methodology of developing product specific interlayer dielectric polish processes. Sahota et al illustrates in Fig. 4, the polishing of a first wafer and measuring the topography of that first wafer, then using the first data points to polish a subsequent wafer. Topography (surface profile measurements) is discussed in col. 17 lines 18-26 and col.15 lines 45-67.

The motivation to modify the teachings of Nagahara et al is to enhance the capabilities of the apparatus from the application of pressure to a specific wafer to wafers in an entire lot or batch. The combined teachings of Nagahara et al and Sahota et al will increase throughput and the uniformity of polishing with a lot of wafers.

3. Claims 1-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Korovin et al(US 6,390,905) in view of Sahota et al (US 5,665,199).

Korovin et al teaches providing CMP using a workpiece carrier with adjustable pressure zones and barriers.

Re Claims 1, 8, 9: The method of Korovin et al teaches selectively applying a plurality of different amounts of pressure to different, selected locations of a backside of the semiconductor device structure and a polishing or planarizing at least one layer of the surface of the semiconductor device structure, see abstract and Figs. 2 and 4.

Re Claim 6, 13, and 14: The different amounts of pressure are provided by biasing independently movable pressurization structures (plenums), see abstract and col. 6.

Re Claims 2,7, 11, 12:The polishing discussed in Korovin et al is CMP according to the title.

Re Claim 10: The selectively applying a plurality of different amounts of pressure and the polishing or planarizing together effect the formation of a substantially planar surface on the semiconductor device structure, see the abstract and col. 6 lines 8-29.

Re Claims 4, 5: At least one raised surface has been located and the adequate pressure applied to planarize see col. 6.

Re Claim 14: The polishing of Korovin et al comprises forming a substantially planar surface on the semiconductor device structure, see abstract.

Korovin et al fails to polishing a second semiconductor structure based on the applied pressure of the first.

Sahota et al teaches a methodology of rdeveloping product specific interlayer dielectrid polish processes. Sahota et al illustrates in Fig. 4, the polishing of a first wafer and measuring the topography of that first wafer, then using the first data points to polish a subsequent wafer. Topography (surface profile measurements) is discussed in col. 17 lines 18-26 and col.15 lines 45-67.

The motivation to modify the teachings of Sommer is to enhance the capabilities of the apparatus from the application of pressure to a specific wafer to wafers in an entire lot or batch. The combined teachings of Korovin et al and Sahota et al will increase throughput and the uniformity of polishing with a lot of wafers.

Response to Arguments

4. Applicant's arguments with respect to claims 1-14 have been considered but are moot in view of the new ground(s) of rejection. The prior art of Nagahara et al, Korovin et al, and Saka et al all teach a method of polishing wherein a force gradient is created from a plurality of immediately distinctly different amounts of pressure as introduced in the amendment to the independent claims.

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sylvia R. MacArthur whose telephone number is 571-272-1438. The examiner can normally be reached on M-F during the hours of 8:30 a.m. and 5 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Parviz Hassanzadeh can be reached on 571-272-1435. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RAM N. KACKAR, P.E.
PRIMARY EXAMINER

Sylvia R MacArthur
Patent Examiner
Art Unit 1763

October 2, 2006